**PH231 Endsemester exam.A – Spring 2021 [50]  
Prerequisite:**You must have a working LTSpice simulation and physical implementation of a waveform **F**unction **G**enerator (FG) that swings to both positive and negative voltages, as used in previous labs.

The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Add a 100μF (electrolytic) capacitor from VCC to GND for the FG, and for the all other active modules involving BJT’s, both in simulation and the built circuit. As discussed in lecture session, this prevents VCC fluctuations caused by FG BJT’s switching  
Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

Stop time = 101m

Time to start saving data = 100m

Maximum time step = 0.01m

This skips the initial transients in the first 100ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of Vin @ *f~ 1kHz*

**Exam.A Increase gain of voltage amplifier**

Fig 1 shows the final design of a Common Emitter voltage amplifier from Lab 4. Use the component values shown in Fig 1 as the starting point for your design in this endsem assignment. You may have used different base bias resistor values & Cin­, Cout in your own solution – please replace those with the standardized values shown in Fig 1

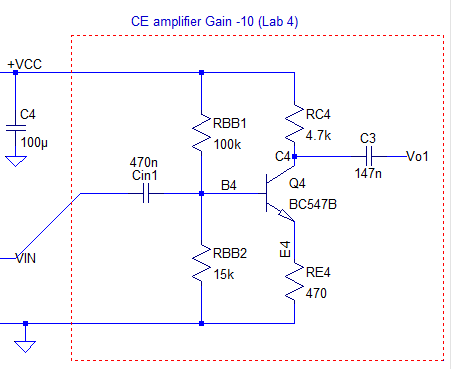


Fig 1: CE voltage amplifier  
(model solution for Lab 4)   
Use this as the starting point for this exam:

Design specifications used to arrive at this design were:

1. Assume VCC = 9V constant,   
   and Q1*β* = 300
2. Use IQ = 1mA
3. Circuit gain = **–10**
4. high-pass *f3dB* = 100 Hz
5. *vin =* ± 0.3V *@* 1.17 kHz

**Level 1 Analyze and determine limits of performance 5   
(revision Lab 4)**

Implement the above circuit model in LTSpice. You can answer the following questions using a combination of LTSpice simulation results and pen+paper calc

1. At the Q point (*vin = 0)* what are the node voltage values at the BJT Q4 terminals? **1**

|  |  |  |
| --- | --- | --- |
| VB|Q | VCQ | VE|Q |
| 1.15V | 4.12V | 0.44V |

[explanatory note, not a question]:   
As you may remember the design sequence for the Q-point is:

* 1. set VC at ~½VCC to ensure maximum possible swing of *vout*
  2. set VE at ~ 0.05 - 0.1VCC ensuring that for chosen value of ICQ, RE dominates over *re*
  3. this gives VB at Q-point required for forward active operation.   
     Apart from the DC value at B of VB|Q the input *vin* is applied at B, hence the voltage at B is VB=VB|Q +*vin*(t). So we should have a clear idea of what is the range of voltage variation allowed at B, such that the BJT always remains forward active.

The following questions guide you towards the correct answer:

1. What are the allowed Upper and Lower limits of VB to keep Q4 forward-active?  
   Upper limit voltage allowed for VB? \_\_2.45V\_\_\_\_ **1**  
   Lower limit voltage allowed for VB? \_\_0.225V\_\_\_\_  
   1. What happens to VC when VB *exceeds* upper limit?
   2. What happens to VC when VB *falls below* the lower limit?
2. You have designed the circuit for ICQ = 1mA. What is the actual value of ICQ obtained with the component values used in the design? **1**1.1mA
3. What is IB at the Q-point? **1**  
   Keep in mind that this will be different in the simulation and the practically built circuit: the simulated model uses BC547B (easy to include in LTSpice) whereas in the breadboard circuit we use BC107   
   -0.1mA
4. With the above voltage & current parameters and the chosen passive component values what is the voltage gain expected from the circuit? Give your derivation with all the relevant formulae and the approximations/assumptions made: **1**

𝑣𝑜𝑢𝑡 = −𝑅𝐶𝑖𝐶

𝑖𝑒=𝑣𝐸𝑅𝐸~𝑣𝐵𝑅𝐸 𝑠𝑖𝑛𝑐𝑒 𝑉𝐵𝐸 = 0.7V 𝑖𝑠 𝑓𝑖𝑥𝑒𝑑 (setting *re+RE ~ RE*)

𝑈𝑠𝑖𝑛𝑔 𝑣𝐵=𝑣𝑖𝑛 𝑎𝑛𝑑 𝑖𝐶=𝑖𝐸 𝑤ℎ𝑒𝑛 𝛽 𝑖𝑠 𝑙𝑎𝑟𝑔𝑒

We combine the above equations to get: 𝑣𝑜𝑢𝑡 = −𝑅𝐶(𝑖𝐸)= −𝑅𝐶(𝑣B/𝑅𝐸)=−(𝑅𝐶/𝑅𝐸)𝑣𝑖𝑛

**Level 2.A Increase AC gain (concept crack) 10**

As discussed in the session notes, the main thing preventing us from reducing the denominator in gain is that we must keep . It’s the reason why was put in the emitter leg in the first place!

1. What component can be **added** to the circuit such that terminal voltages of Q4 at DC remain unaffected, and yet we can analyze the AC behavior independently?

A capacitor Cnew can be added parallel to RE between the emitter and the ground.

1. With correct answer to question 1, it would be logical next step to add another component that comes into play only in AC operation. This component, in combination with allows us to set the gain G of the amplifier while staying safely above the limit  
   What is this 2nd component to be added?   
   Combine the answers to question 1 & 2 and draw a circuit fragment here of what goes between the Q4 – emitter and GND by adding these two components [TWO components are required to be added to Fig 1: you have to figure what they are, and how to connect them]

A resistor RE1can be added in series with the above mentioned capacitor.

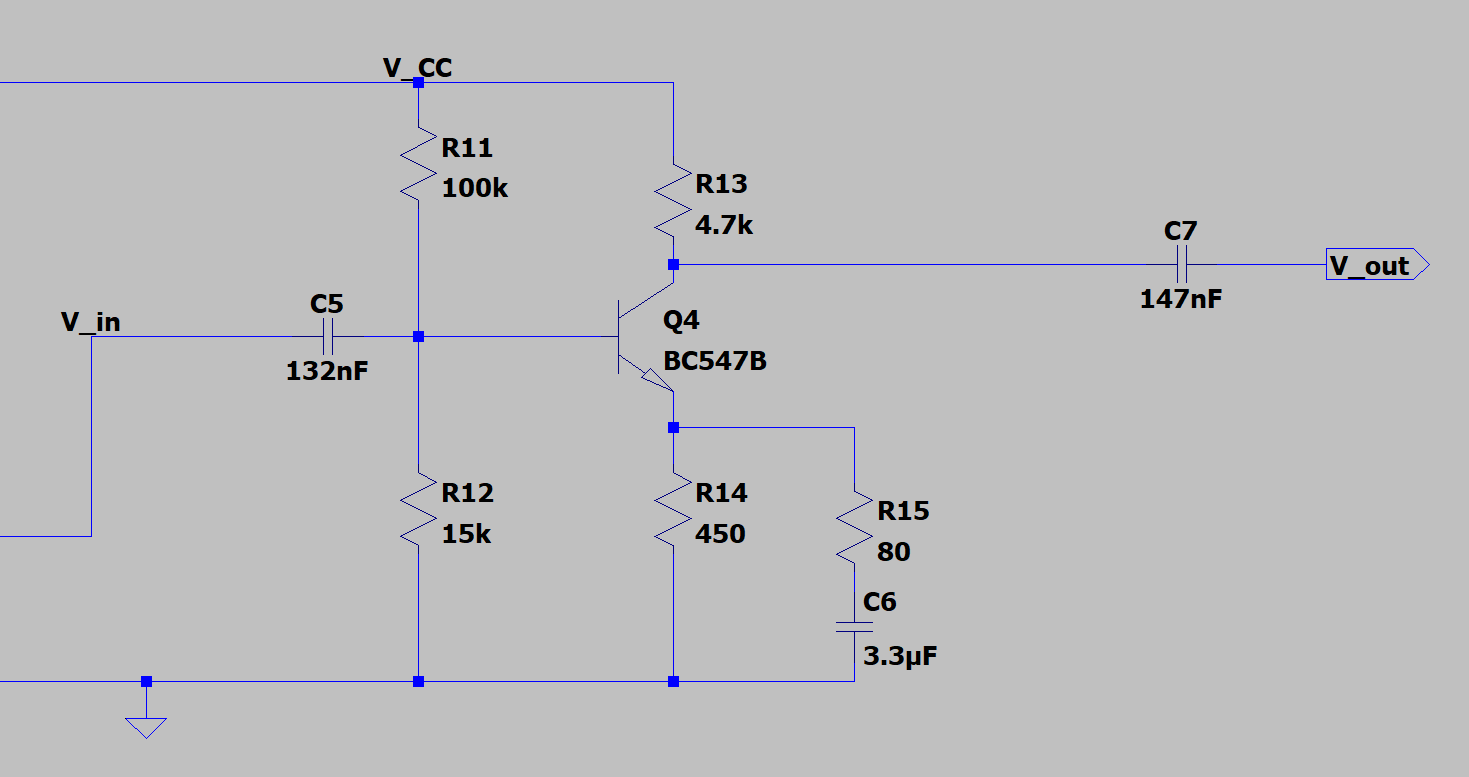
1. What are the design constraints that lead you to calculate the values of components you have chosen to add in answer to question 1 & 2 above?  
     
   Cnew = 1/ (2πfR) = 3.3µF

𝑅𝐸 || 𝑅𝐸1 >> re

**Level 2.B Increase AC gain (design implementation) 5**

Redesign the CE voltage amplifier of Fig 1 using the conceptual additions of Level 2.A to have a new set of design specifications:

1. Assume VCC = 9V constant,   
   and Q4*β* = 300
2. Use IQ = 1mA
3. Circuit gain = **–50** → gain is 5× higher!
4. high-pass *f3dB* = 100 Hz



**Level 3 High gain voltage amplifier**

**3.A) Circuit simulation [5]**

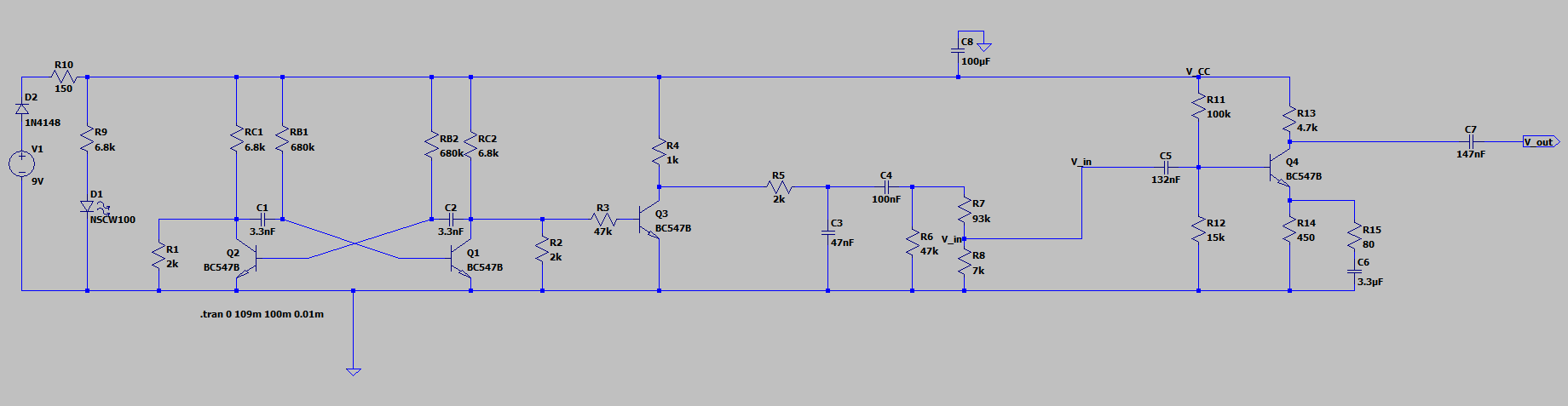
Make an LTSpice circuit simulation of your re-designed high voltage gain amplifier as per calculations of Level 2.B

1. Start with the standard FG simulation as published on Moodle.
2. Add the high voltage gain CE amplifier as a separate module, taking its *v­­in* from the output of the FG potentiometer

Add a 100μF bypass capacitor between VCC and GND as discussed in class, for both the FG

and CE amplifier modules to reduce unwanted transients in Vcc supply.

Put your LTSpice circuit diagram here **1**



Simulation results: (use the following LTSpice simulation parameters)

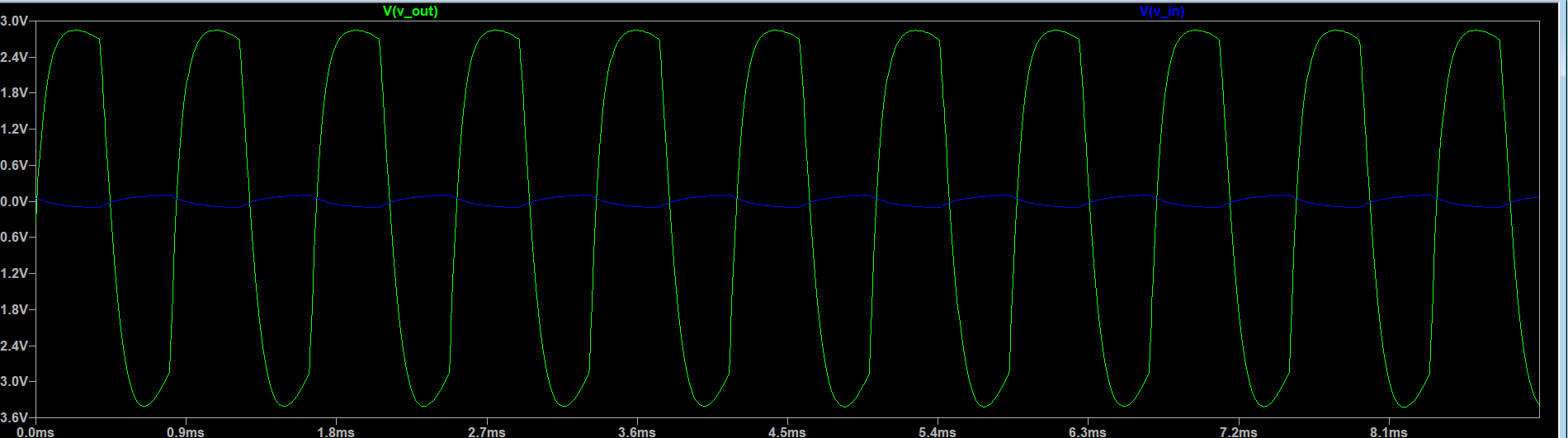
Stop time = 101m

Time to start saving data = 100m

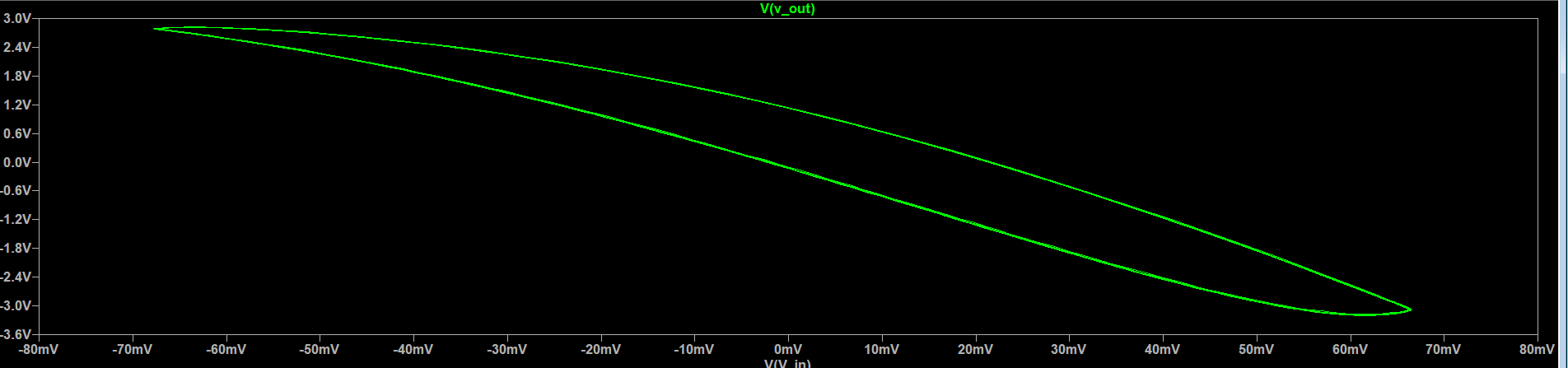
Maximum time step = 0.01m

Run the simulation and provide two output plots below:

**Plot 1)** *vin*(t) and *vout*(t) voltages (to be compared with experimental observations)  
Typically you read off the peak values of the two voltages and decide the gain is the ratio of those voltages – this is not fully correct! **2**



**Plot 2)** *vout*(t) *v/s vin*(t) demonstrating expected *linear* voltage gain. Plotting the ratio of *vout*(t)to *vin*(t) *throughout* the range of variation gives you a much clearer idea of the gain linearity (*vin* and *vout* are out of phase, so comparing just the peak values includes unwanted factors in the ratio) **2**

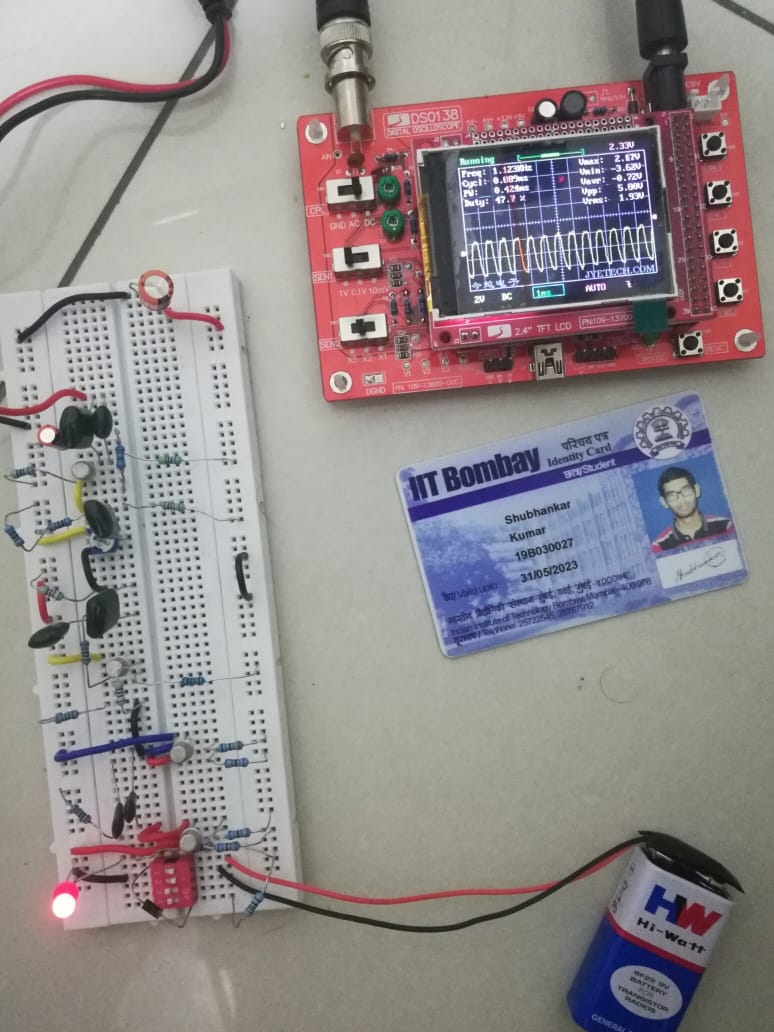
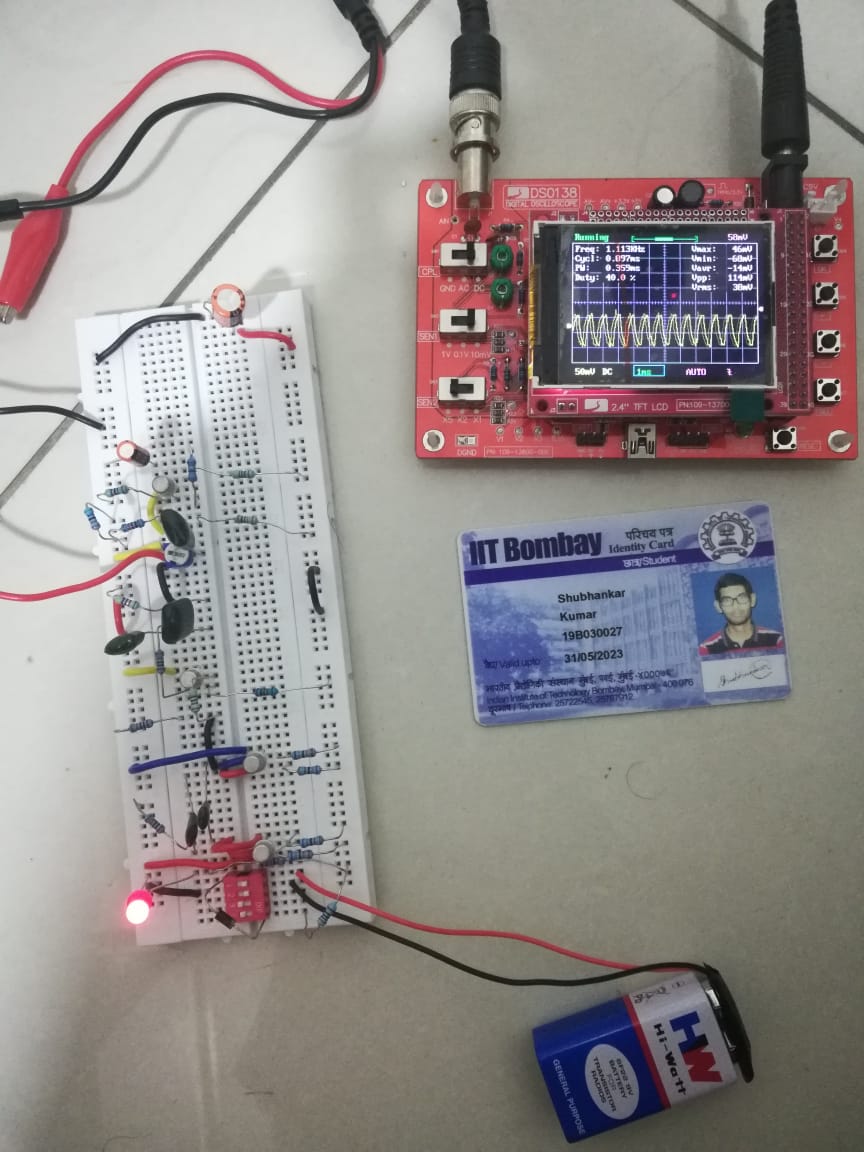


**3.B) Hardware demo: [25]**

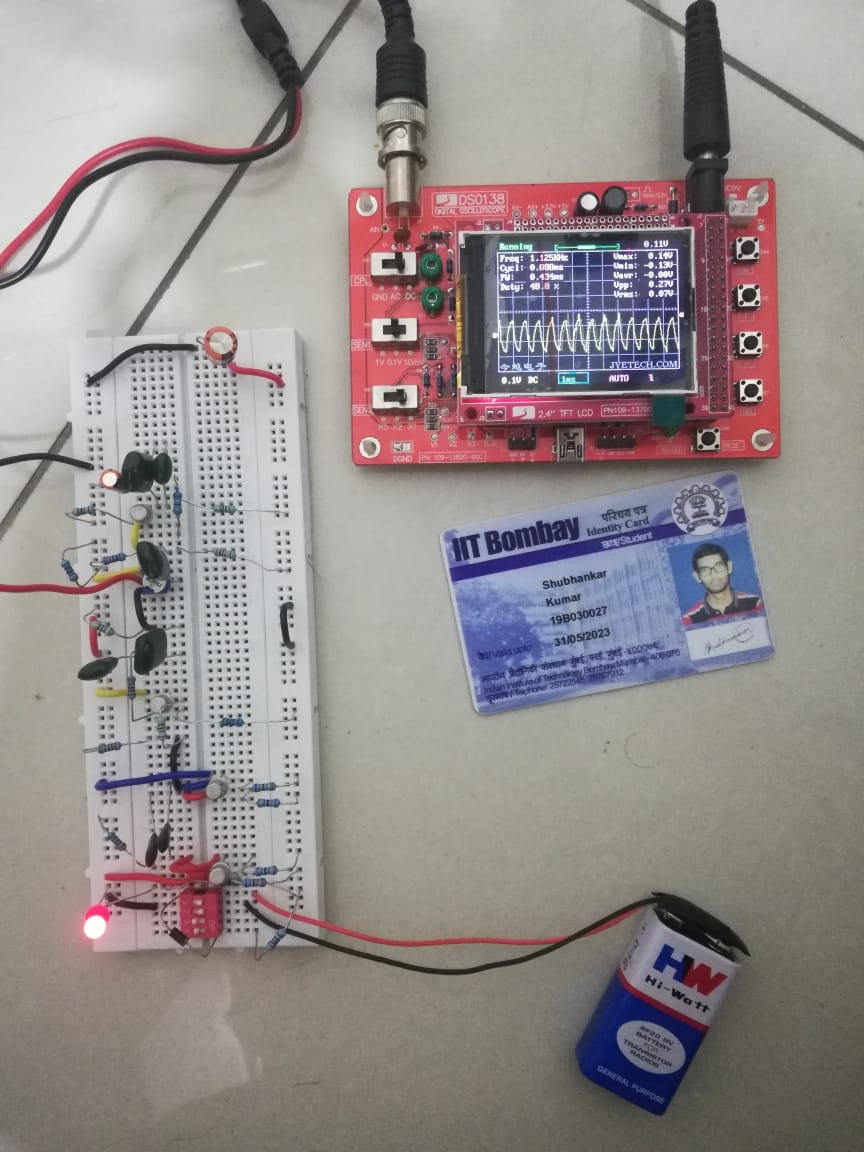
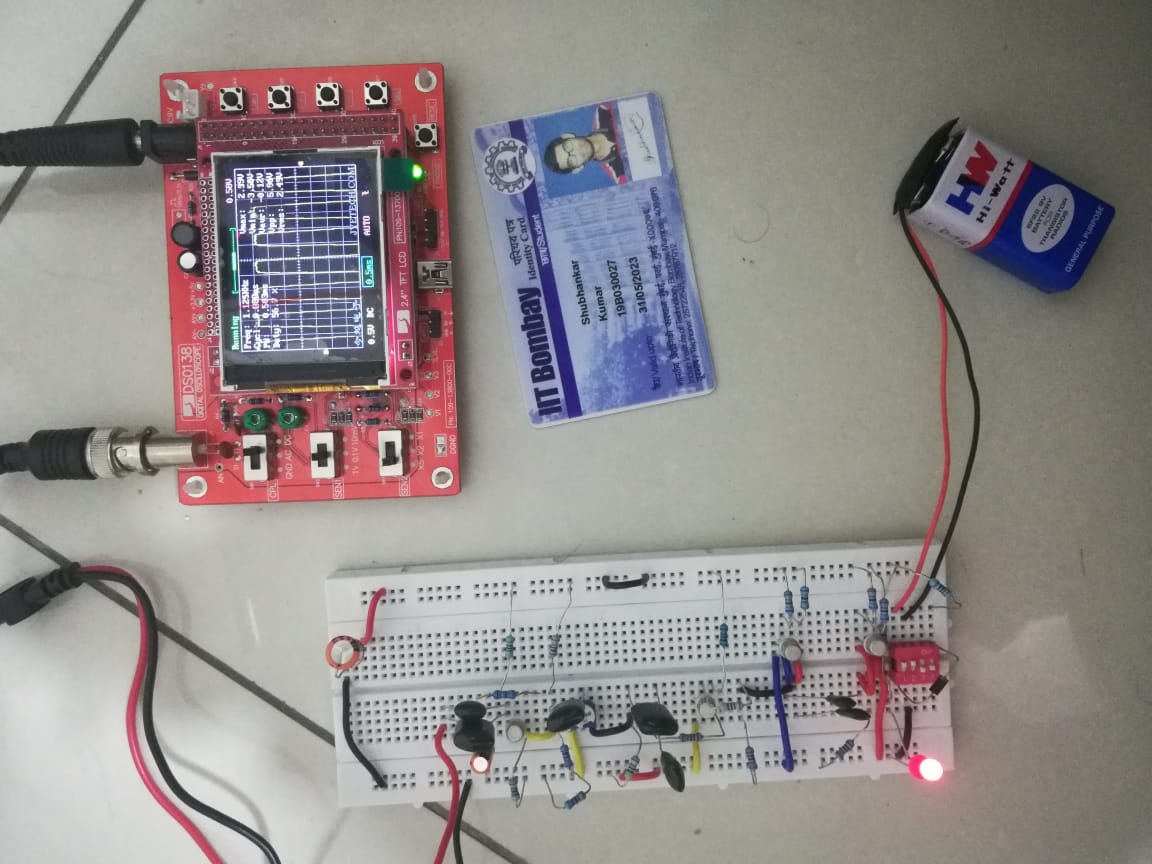
Build the re-designed high gain CE voltage amplifier circuit of Level design on your breadboard. Adjust the FG output through the 100k potentiometer to obtain a desired range of *vin* to your voltage amplifier.

Put in photos of your successful demo below. Each photo must contain your circuit, the DSO trace measurement and your ID card:   
Since the DSO has only one channel measurement, label each photo indicating which measurement is *vin* and which one is *vout*

1. *vin* amplitude set to a (very small!) value such that you get   
   *vout ~ G×vin* with *G ~ –50*2 photos expected: 1 of *vin* and 1 of *vout* **20**

   
VIN  VOUT

1. *vin* amplitude *increased* to a value such that *vout* starts showing non-linearity similar to the type diagnosed in Level 1 **5**  
   2 photos expected: 1 of *vin* and 1 of *vout*use arrows and text labels overlaid on your photo indicating where the BJT goes into saturation or cutoff.

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Square peaks indicate cutoff/saturation